WHAT IS CLAIMED IS :

1. A semiconductor integrated circuit testing method comprising the steps of:

causing a tester to generate a measuring signal to all pins of a semiconductor integrated circuit;

generating a trigger signal;

latching said measuring signal by use of said trigger signal;

storing the latched measuring signal as data into storing means; and

reading the stored data from said storing means for output to said tester.

2. The semiconductor integrated circuit testing method according to claim 1, wherein the data stored into said storing means represent electric lengths of all pins of said semiconductor integrated circuit.

3. The semiconductor integrated circuit testing method according to claim 1, further comprising the step of creating a calibration data file based on the data sent to said tester.

4. The semiconductor integrated circuit testing method according to claim 3, further comprising the step of referencing said calibration data file to correct waveform timing of said measuring signal upon functional test performed by said tester.

5. The semiconductor integrated circuit testing method according to claim 1, wherein said trigger signal is a high-speed clock signal.

6. The semiconductor integrated circuit testing method according to claim 1, wherein said trigger signal is selected from among a plurality of signals generated with different delay times

on the basis of a low-speed clock signal.

7. A semiconductor integrated circuit testing apparatus comprising correcting means for correcting input waveform timing of a measuring signal applied to all pins of a semiconductor integrated circuit.

8. The semiconductor integrated circuit testing apparatus according to claim 7, wherein said correcting means includes:

clock generating means for generating a clock signal;

latching means for latching said measuring signal by use of said clock signal from said clock generating means;

storing means for storing as data said measuring signal latched by said latching means; and

controlling means for retrieving the data held in said storing means for output to an external entity.

9. The semiconductor integrated circuit testing apparatus according to claim 8, wherein said latching means, said storing means and said controlling means are incorporated in said semiconductor integrated circuit.

10. The semiconductor integrated circuit testing apparatus according to claim 8, wherein said latching means is constituted by terminating circuits and latch circuits, and said storing means by FIFO memories and scan FF circuits.

11. The semiconductor integrated circuit testing apparatus according to claim 8, wherein said clock generating means is a high-speed clock generating circuit for generating a high-speed clock signal.

12. The semiconductor integrated circuit testing apparatus according to claim 8, wherein said clock generating means includes:

a low-speed clock generating circuit for generating a low-speed clock signal;

a delay circuit for generating a plurality of signals with different delay times on the basis of the output from said low-speed clock generating circuit; and

a selection circuit for selecting one of said plurality of signals from said delay circuit.

13. The semiconductor integrated circuit fabricated by use of a semiconductor integrated circuit testing method according to claim 1.

14. The semiconductor integrated circuit fabricated by use of a semiconductor integrated circuit testing apparatus according to claim 7.